Claims Amendments

Please replace the previous claims with the claims listed below.

Claims 1-67 (canceled)

68. (previously presented) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data from a received signal, which comprises capturing multiple samples of the signal per a symbol time with a sampling clock or its sub-clocks defining known phase displacements versus the sampling clock; the DSP MSP method comprising the steps of:

detection of phases of rising and falling edges of the signal by using said signal samples captured at said known phase displacements;

evaluation of a length of a pulse of the signal by using said phases of signal edges;

calculation of a number of data bits received in the pulse by using said evaluation of the pulse length.

69. (currently amended) A method as claimed in claim 68, comprising use of multiple sequential processing stages or parallel processing phases of said captured samples; wherein:

said sequential processing stages are driven by the sampling clock or clocks synchronous to the sampling clock;

consecutive said parallel processing phases are driven by clocks which are shifted in time by corresponding consecutive periods of said sampling clock and have 2 or more times lower frequencies than a frequency of the sampling clock, in order to multiply processing times assigned for said parallel phases;

outputs of a one parallel processing phase are passed to a next parallel phase, wherein output register bits of the original parallel phase are re-timed by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase;

said passed outputs are used by a following sequential processing stage which belongs to the next parallel processing phase.

Claims 70-87 (canceled)

88. (new) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data
   from a received signal, which comprises capturing multiple samples of the signal per a symbol time
   with a sampling clock or its sub-clocks defining known phase displacements versus the sampling
   clock; the DSP MSP method comprising the steps of:

detection of phases of rising and falling edges of the signal by using said signal samples captured at
       said known phase displacements;

measurement of a length of a pulse of the signal occurring between said phases of signal edges, based
       on a known relation between a frequency of the sampling clock and a frequency of a received
       signal clock;

evaluation of a number of data bits received in the pulse, based on said measurement of the pulse
       length.

89. (new) A method of digital signal processing of multi-sampled phase (DSP MSP) for recovering
   data from a received signal, the DSP MSP method comprising the steps of:

maintaining a known frequency relation between a sampling clock and a received signal clock;

detection of phases of rising and falling edges of the signal by using the sampling clock or its sub-
       clocks defining known phase displacements versus the sampling clock;

measurement of a length of a pulse of the signal occurring between said phases of signal edges, based
       on such known frequency relation;

evaluation of a number of data bits received in the pulse, based on said measurement of the pulse
       length.

90. (new) A method of digital signal processing of multi-sampled phase (DSP MSP) for recovering
   data from a received signal, the DSP MSP method comprising the steps of:

producing a sampling clock which maintains a frequency alignment with a received signal clock;

detection of phases of rising and falling edges of the signal by using the sampling clock or its sub-
       clocks defining known phase displacements versus the sampling clock;

measurement of a length of a pulse of the signal occurring between said phases of signal edges, based
       on such frequency alignment;

evaluation of a number of data bits received in the pulse, based on said measurement of the pulse

        length.

91. (new) A method of digital signal processing of multi-sampled phase (DSP MSP) for recovering

    data from a received signal, the DSP MSP method comprising the steps of:

measurement of a frequency relation between a sampling clock and a received signal clock;

detection of phases of rising and falling edges of the signal by using the sampling clock or its sub-

        clocks defining known phase displacements versus the sampling clock;

measurement of a length of a pulse of the signal occurring between said phases of signal edges,

        utilizing such measured frequency relation;

evaluation of a number of data bits received in the pulse, based on said measurement of the pulse

        length.